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Abstract

Solid-state pulsed power topologies are a rapidly evolving field due to the speed at which semiconductor voltage handling improves. One popular generator is the Linear Transformer Driver (LTD), a derivation of the Inductive Voltage Adder (IVA) where the driving circuitry is located internally instead of externally like IVAs. While they do utilize magnetic cores, their main advantage is their stage-to-stage isolation (each stage ground referenced), which allows for simple low-voltage triggers. These devices are also easily scalable due to their modular design, consisting of multiple axial stages mounted about an inner stalk, with each stage consisting of multiple bricks. The colloquial name, bricks are individual pulser stages typically consisting of a solid-state switch such as a MOSFET, a gate driver, protection circuitry (as needed), and storage capacitors.

A key function of the LTD is their modulation (wave shaping) capability by controlling the on-off times of individual stages, resulting in constructive and destructive interference along the inner stalk. This makes shot-to-shot and even pulse-to-pulse variation possible, tailoring waveforms to specific applications. Expanding these modulation capabilities would allow for increased waveform correction due to common occurrences such as impedance mismatch and system parasitics. While individual stage timing is well documented, control of individual stage voltages would provide more fine control in terms of wave shaping. Since these generators are typically used for their high repetition rates, it is not feasible to change the capacitor charge voltage during the inter-pulse period of a burst (typically hundreds of ns), requiring a different approach. A modified LTD topology is proposed with each brick comprised of multiple switches in a solid-state Marx configuration. This allows for control of each individual switch in the Marx chain, resulting in discrete variable output voltage on a stage-by-stage basis. A circuit model and constructed stage is characterized and presented, denoting added complexities of adopting a more dense topology per brick.

Background

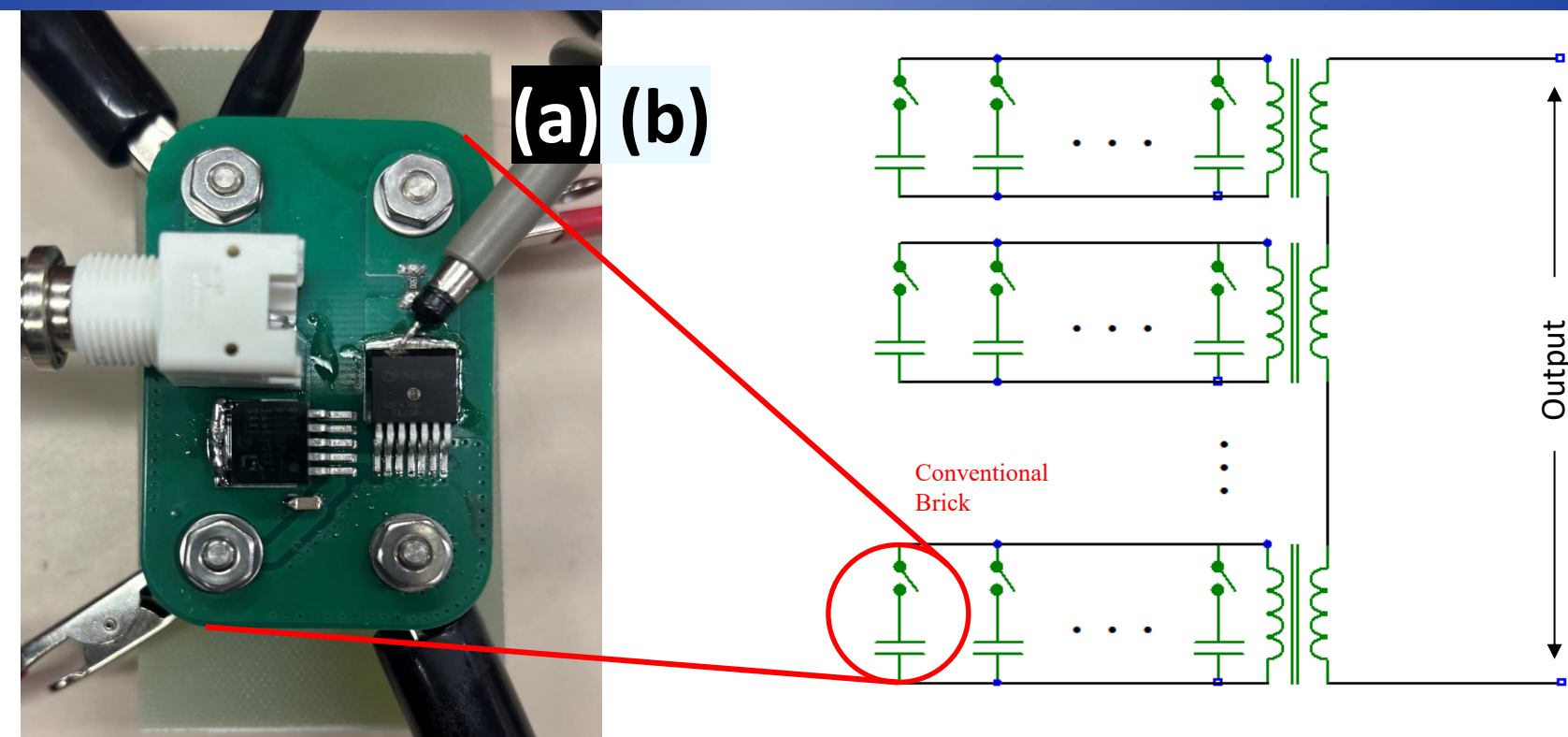


Fig. 1: Left image of a single, traditional SSLTD brick driving a dummy load. Right: simplified circuit diagram of an N-stage (adapted from [1-2])

- A standard solid-state LTD (SSLTD) contains a single switch in series with a charged capacitor. Multiple bricks are added parallel to symmetrically drive the inner stalk based on the current requirements of the system.
- For a traditional SSLTD, the maximum voltage of each stage is ultimately constrained by the voltage holdoff rating of each switch.
- Multi-stage LTDs produce an output voltage $N \cdot V_{charge}$ where N is the number of stages fired. For single switch bricks, the total voltage of system tends to be proportional to the physical size of the system.

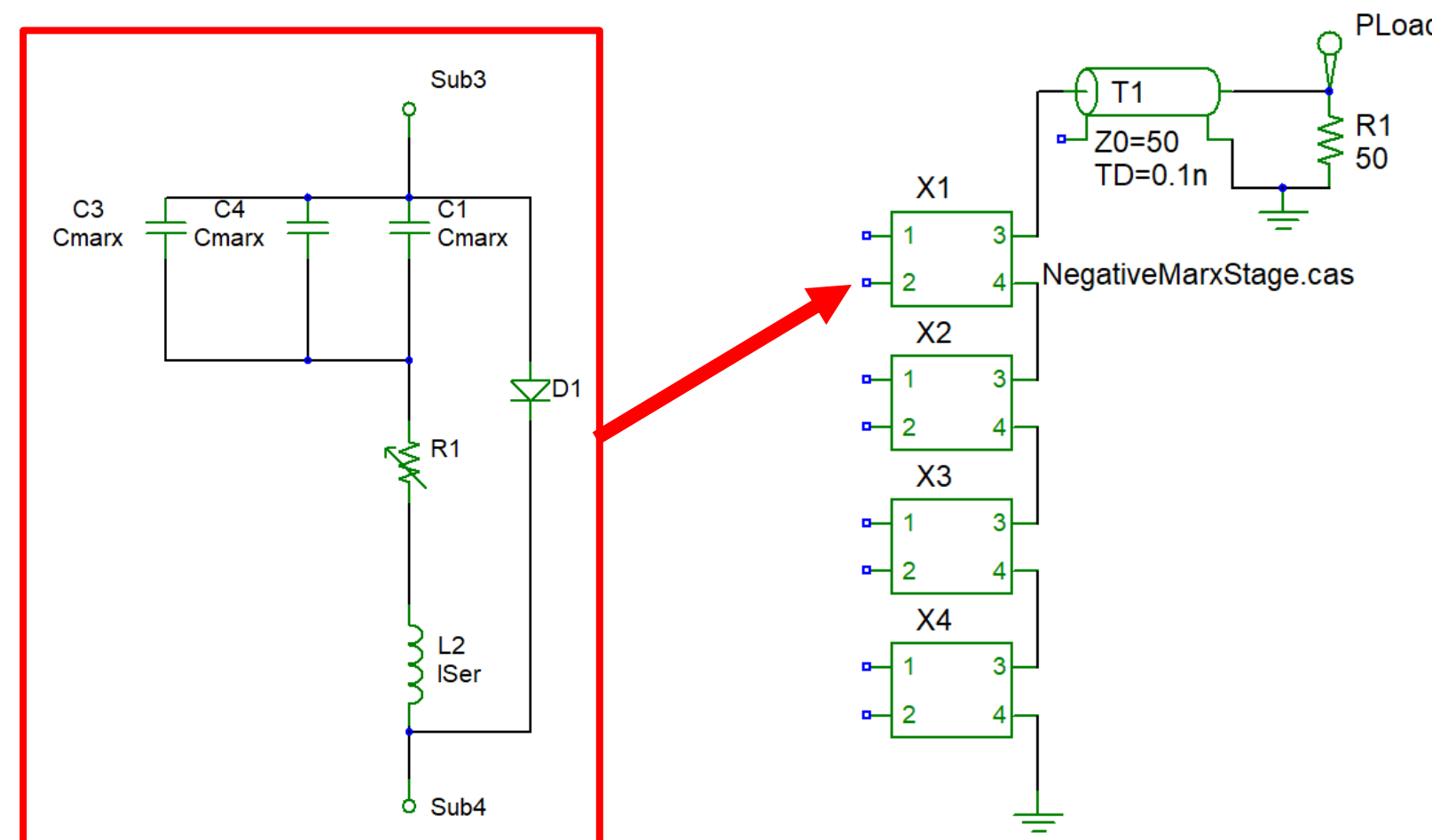


Fig. 2: Simulation circuit model of negative SS Marx topology.

- By integrating multiple Marx cells into a single brick, each switch only handles its local storage-capacitor voltage while the cell outputs add in series to generate a higher total brick voltage. [2-3]
- This allows the proposed Marx-based brick to increase the achievable stage voltage and decrease overall LTD stage requirement (footprint)
- Condensing multiple single switch stages results in increased complexity regarding switching control, referencing, and increased overall breakdown risk.

Simulation Results

Simulations were carried out with an ideal circuit topology for a single brick and a 10-stage LTD-Marx hybrid. Initial modulation optimization algorithm results are also discussed.

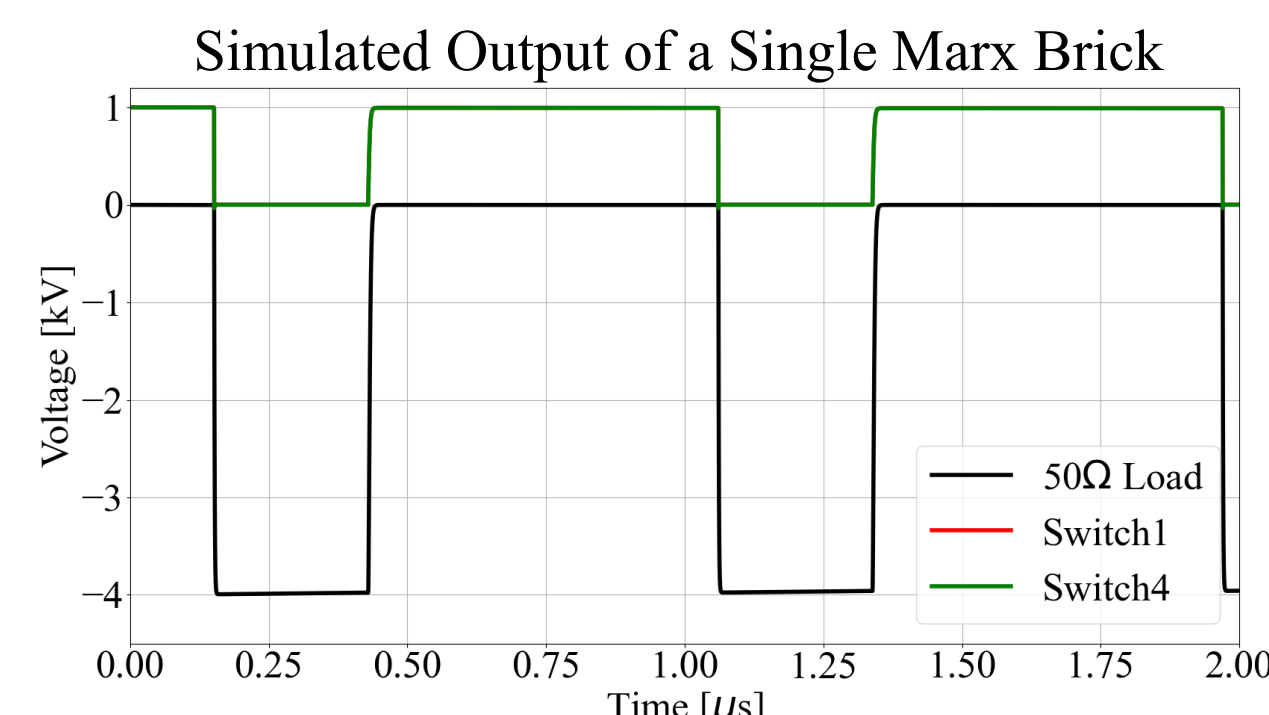


Fig. 3: Marx brick producing 4kV output

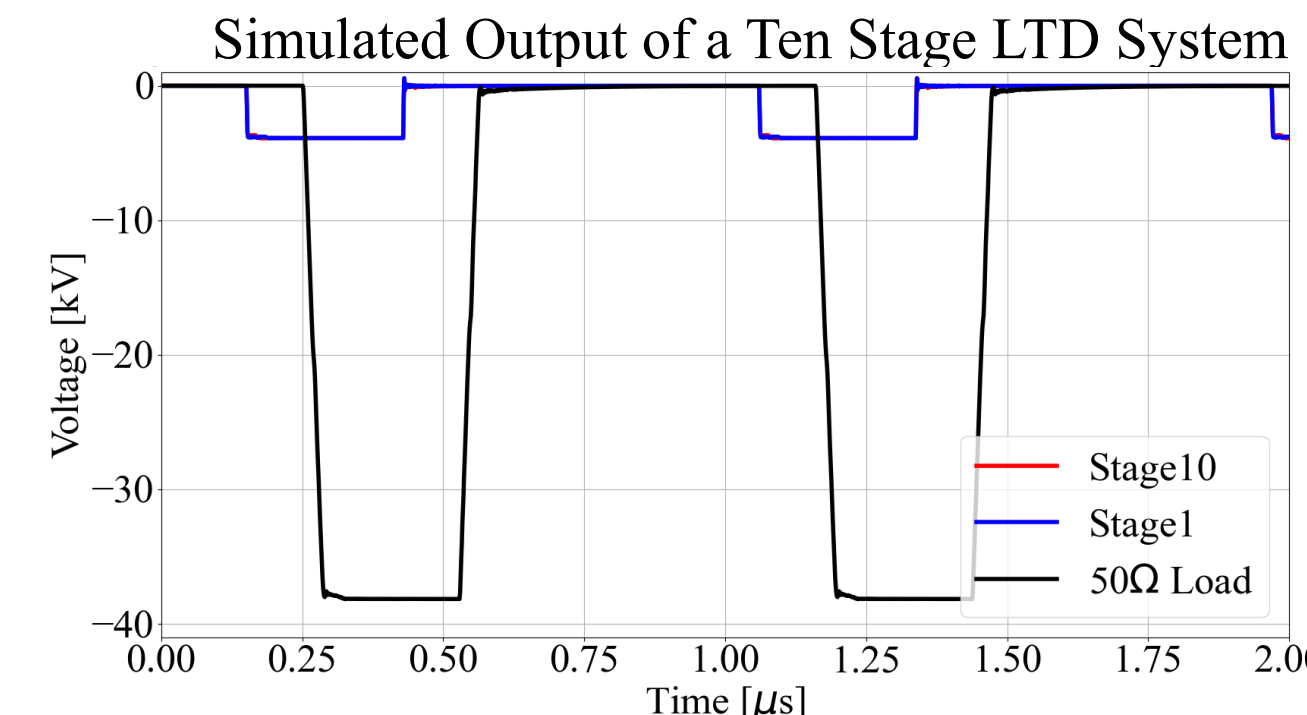


Fig. 4: Ideal, 10-stage LTD-Marx hybrid simulation results

- (Above): Each Marx brick contains four switching cells ($N = 4$), with each cell charged to $1000V$ ($V_{charge} = 1kV$).
- The resulting brick output approaches $N \cdot V_{charge} = 4kV$.
- (Above): A 10-stage LTD configuration was simulated with minor parasitics included (estimated series inductance and core losses).
- 50Ω stalk is terminated into static 50Ω resistive load.

Optimization-Based Waveform Synthesis

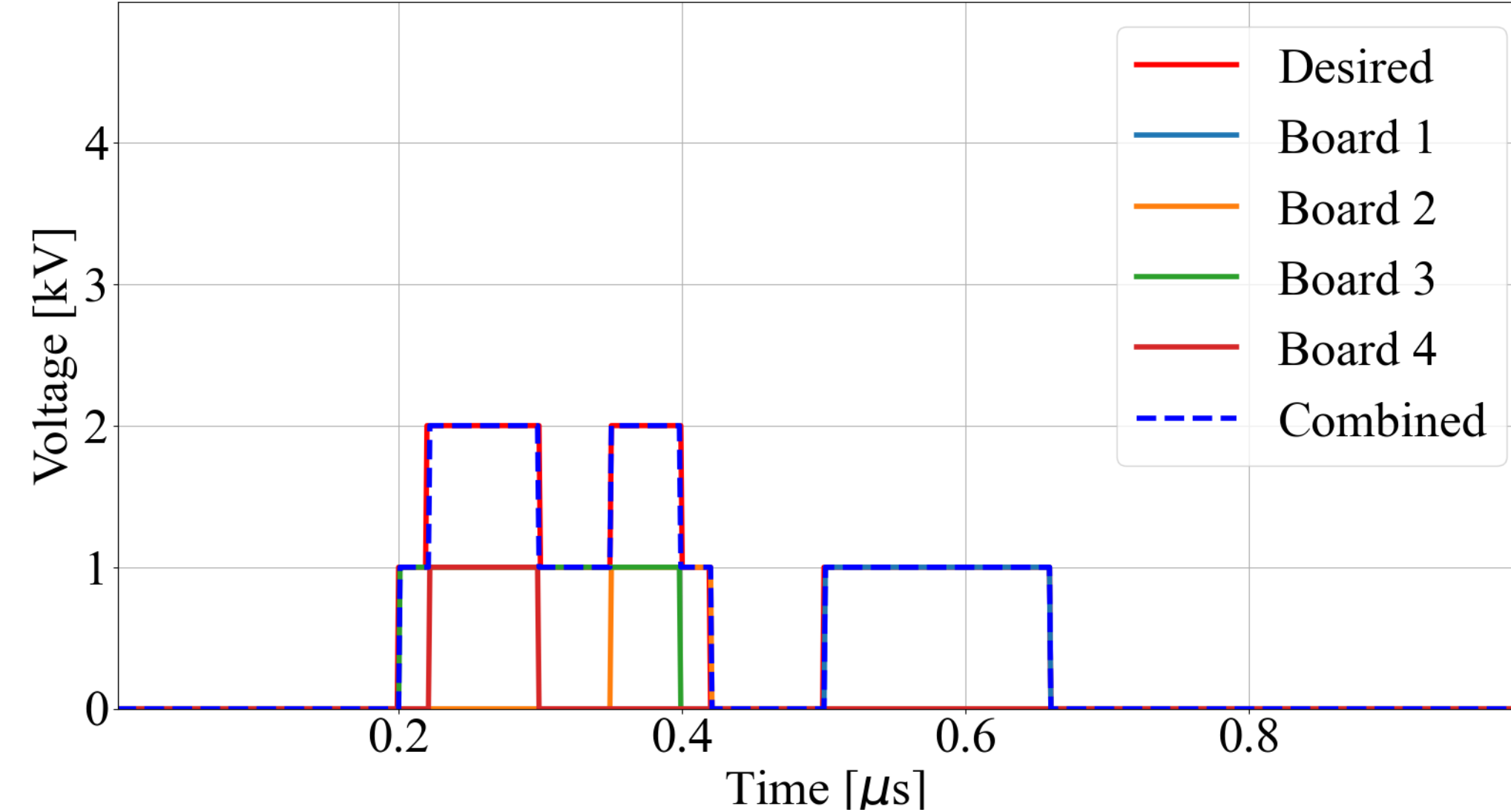


Fig. 5: Optimization routine determines stage contributions (Boards) to result in Desired waveform (red).

- An optimization algorithm using an open-source differential evolution method determined stage contributions required to synthesize desired waveforms.
- Multiple pulse shapes, including separated pulses, were generated using a single Marx stage.
- (Left): The desired waveform (red) is fed to the algorithm, which has control of pulse start time and width.

Experimental Setup

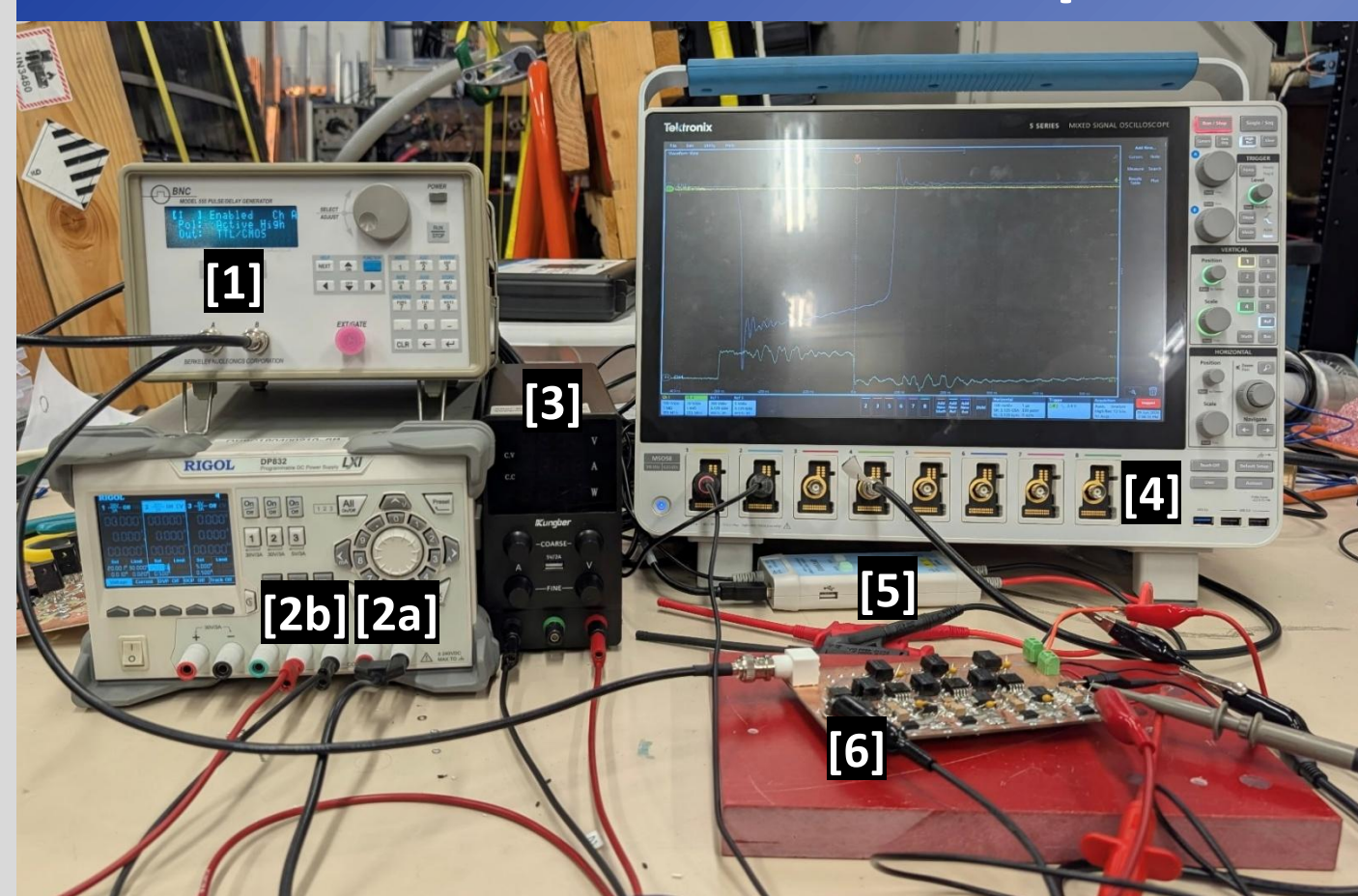


Fig. 6: The test bench used to record experimental data

Prototype Specifications:

- MOSFET: G3F18MT12J-TR
 - V_{DS} Rating: 1200V
 - On State Resistance: 18.5m Ω
 - Capacitor: C2220C164KFRCAUTO
 - Voltage Holdoff: 1500V
 - Nominal Capacitance: 0.16uF
 - Effective capacitance is voltage dependent due to X7R behavior [4]
 - Gate Driver: IXDN609YI
 - Supply Voltage: 24V
 - Peak Source/Sink Drive Current: 9A
- Architecture: For discrete voltage control, power is currently enabled ON/OFF for gate drivers. Conduction path utilizes bottom rung of charging diodes for $N < 4$ stages.

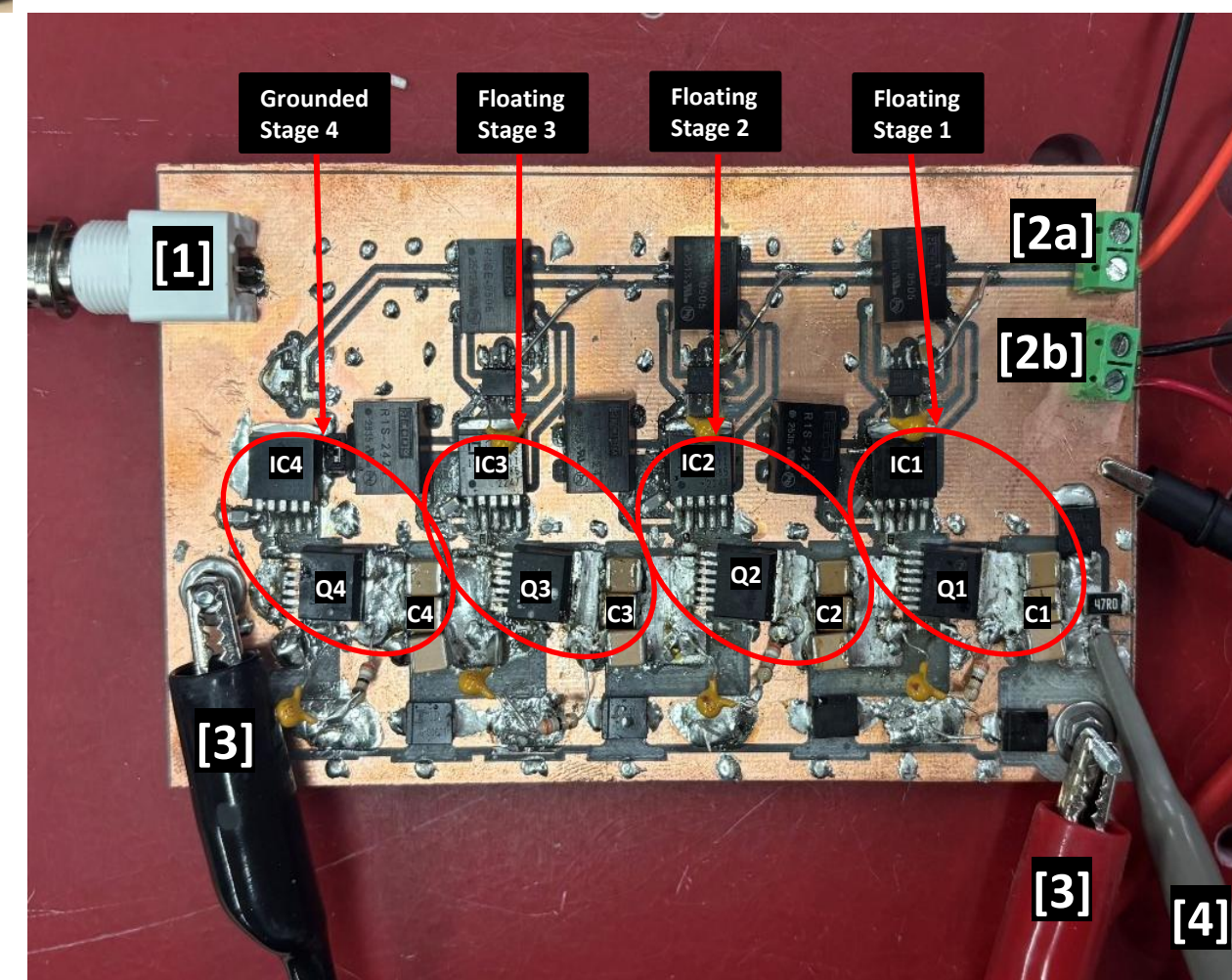


Fig. 7: Single Marx brick denoting individual Marx stages (MOSFETs and Drivers).

Experimental Results

Discrete Marx Stage Control

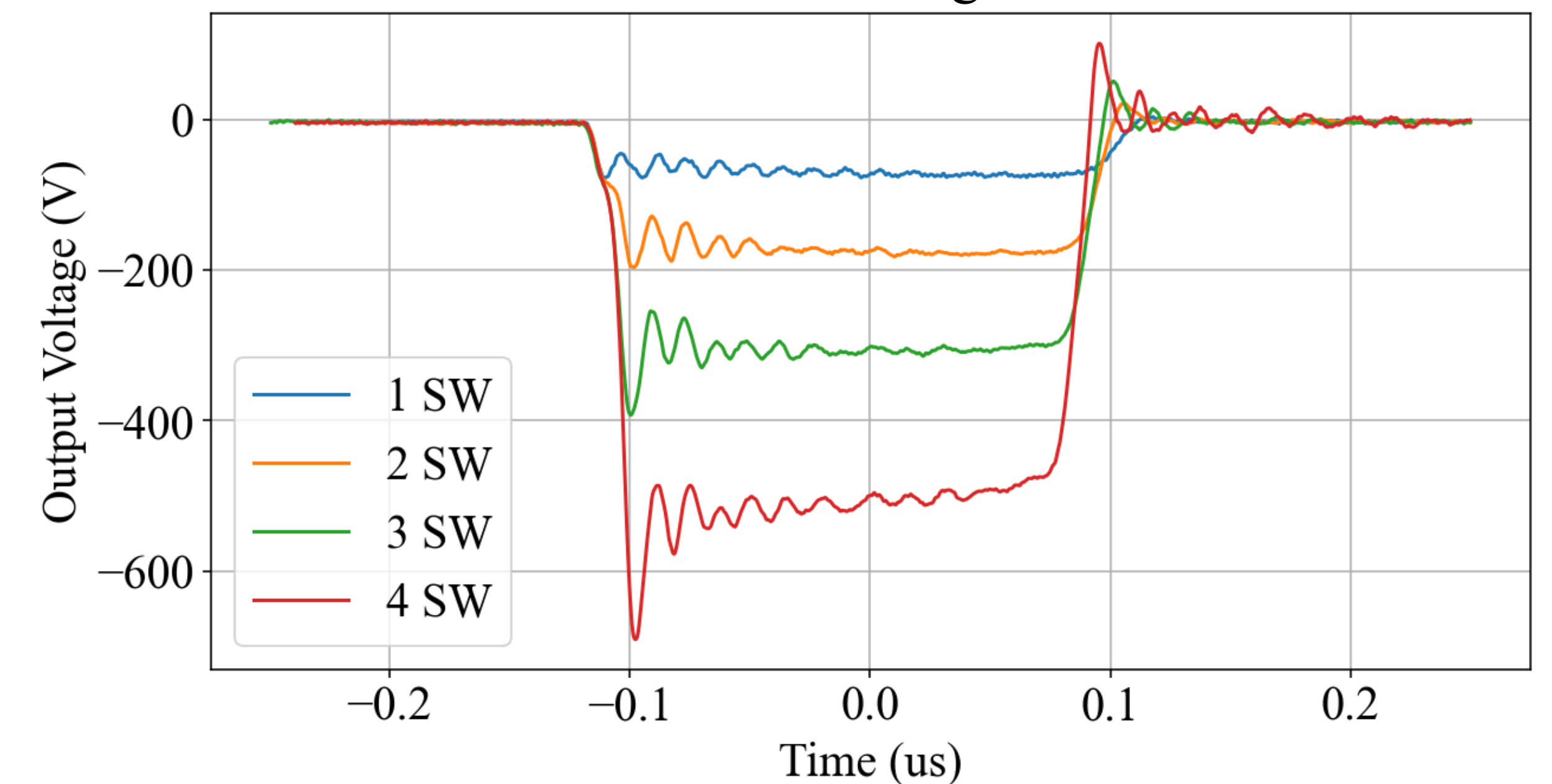


Fig. 8: Output voltage of first trigger demonstrating discrete voltage levels generated through independent Marx-stage activation (150ns pulse width) where 0.0 seconds is falling edge of the final trigger.

- Four discrete output voltage levels were experimentally demonstrated. Fall times are noticeably faster with additional stages. Stages are individually enabled or disabled by cutting power to gate driver power rail.

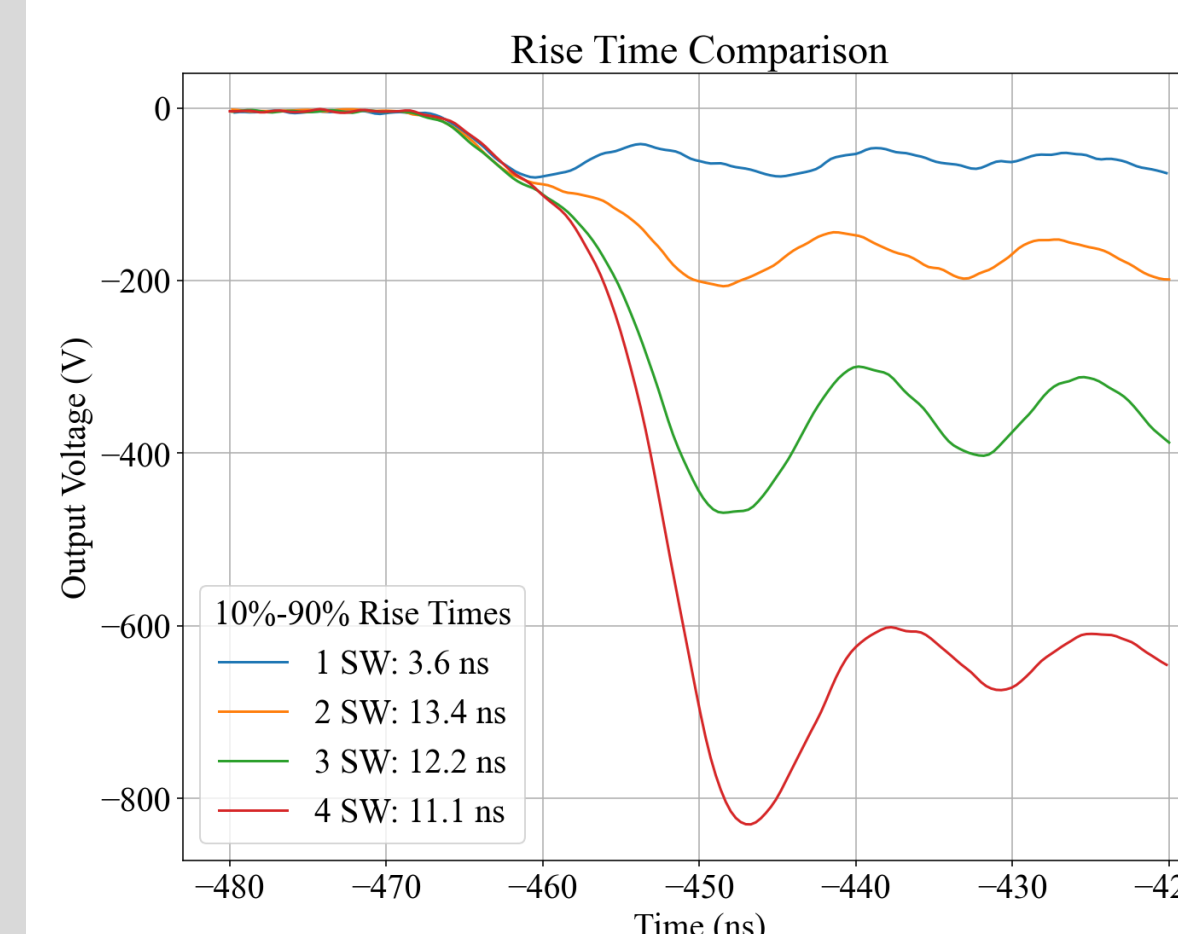


Fig 9. Output Voltage at 10%-90% Rise Times

- Multi-switch operation produced slower rise-times than single-switch operation presumably from series inductance of additional stages.
- More analysis required for prototype characteristics under various loads, and multi-pulse conditions.
- Significant droop is observed during multi-switch operation which follows reduction of overall Marx capacitance with additional stages.

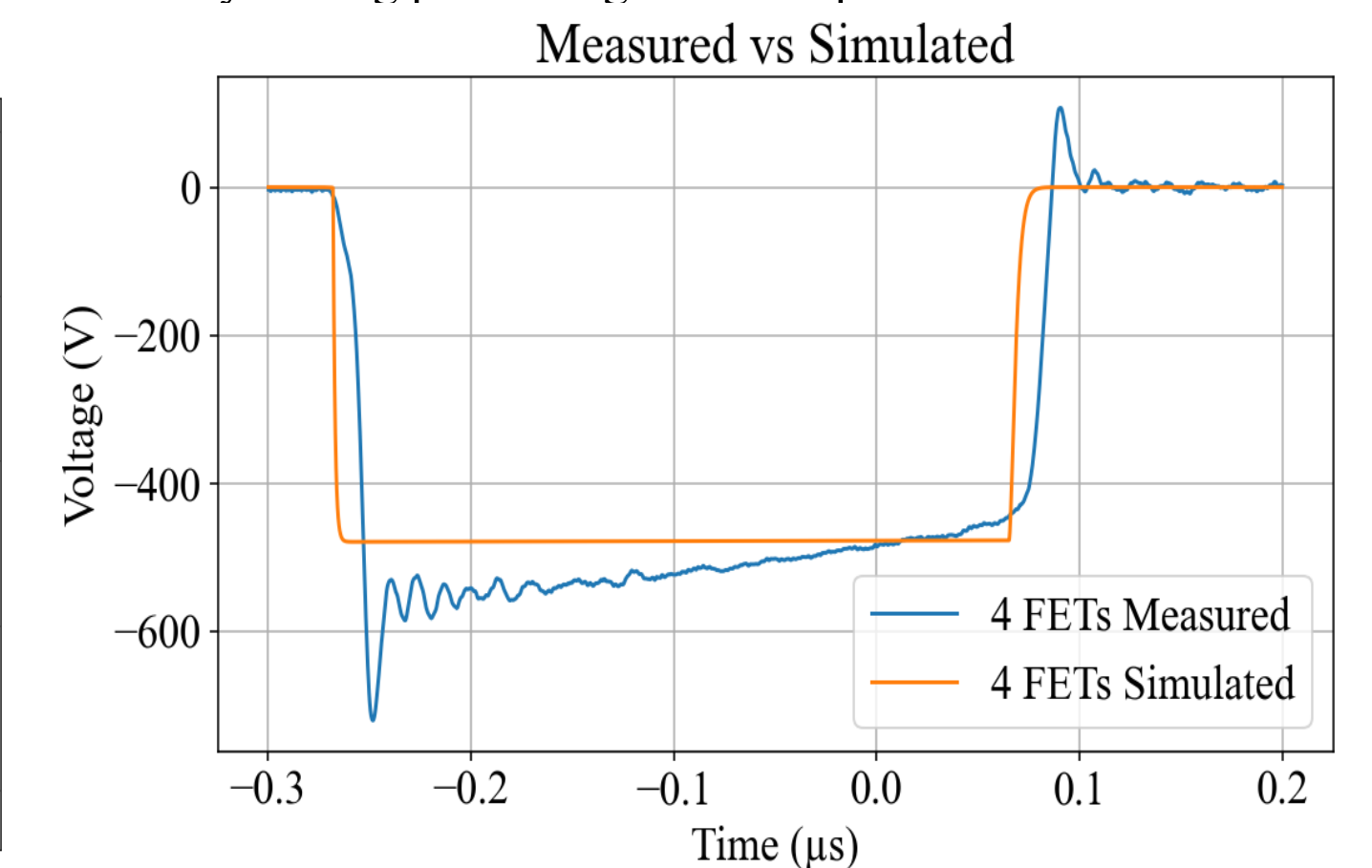


Fig. 10: Experimental vs ideal 4-switch output waveforms (300ns pulse width)

- Overshoot, parasitics, and non-linearity of X7R to be revisited in circuit model.
- Results indicate the ideal simulation currently produces general behavior of prototype stage.
- Future simulations to be coupled to optimization algorithm for modulation.

Conclusions

- A Marx-based, solid-state LTD brick architecture was successfully designed, simulated, and experimentally evaluated.
- Independent stage activation produced four discrete output voltage levels, serving as a proof of concept for modulation control with pulse width and voltage amplitude.
- Experimental measurements show good alignment with first order circuit model utilizing CASTLE [5], which can further be expounded upon by adding parasitics and non-linearities.
- At the cost of additional implementation complexity, the proposed architecture increases the achievable stage voltage compared to a single switch topology, while maintaining a compact LTD footprint.
- The proposed topology introduces discrete stage-voltage control as an additional degree of freedom for modulation beyond conventional LTD timing control.
- Optimization-based waveform synthesis demonstrated the potential for generating desired output waveforms through independent Marx cell control.
- Future work will focus on full-stage implementation, waveform synthesis capabilities, and further comparison with simulation results.

References

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