

The University of Texas at Arlington
Department of Electrical Engineering
EE 4240 — Senior Design II

Design and Implementation of a Solid-State Linear Transformer Driver

Spring 2026 LTD Team

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Final Report

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Abstract

This report documents the design, simulation, and prototype implementation of a solid-state Linear Transformer Driver (LTD) developed as a senior design project at UT Arlington. The system replaces gas-switched architectures with parallel SiC MOSFET bricks, delivering nanosecond pulses at moderate voltages. The trigger chain uses an FPGA with fiber-optic links to isolate the control electronics from the high-energy stage. A first-revision brick (V1) was fabricated and tested on a resistive load. Adding a flyback diode and R-C snubber reduced ringing and improved the waveform. A revised brick (V2) with an integrated snubber footprint and opto-isolated trigger was designed and ordered. This report presents the design decisions, test results, and future work.

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1 Introduction

Pulsed-power systems generate short, high-amplitude pulses by storing energy slowly and releasing it quickly. They are used in applications from fusion research to wastewater treatment. Two common architectures are the Marx generator and the Linear Transformer Driver (LTD).

The Marx generator charges capacitors in parallel and switches them into series. This works but the series stack accumulates parasitic inductance, which limits current rise time [1]. The LTD adds voltage magnetically by stacking cavities along a common axis. Each cavity is short and radially symmetric, which reduces loop inductance and enables faster rise times [2].

This project builds a solid-state LTD using SiC MOSFETs instead of gas spark gaps. Solid-state switches give better repetition rate, less jitter, and lower maintenance than gas switches.

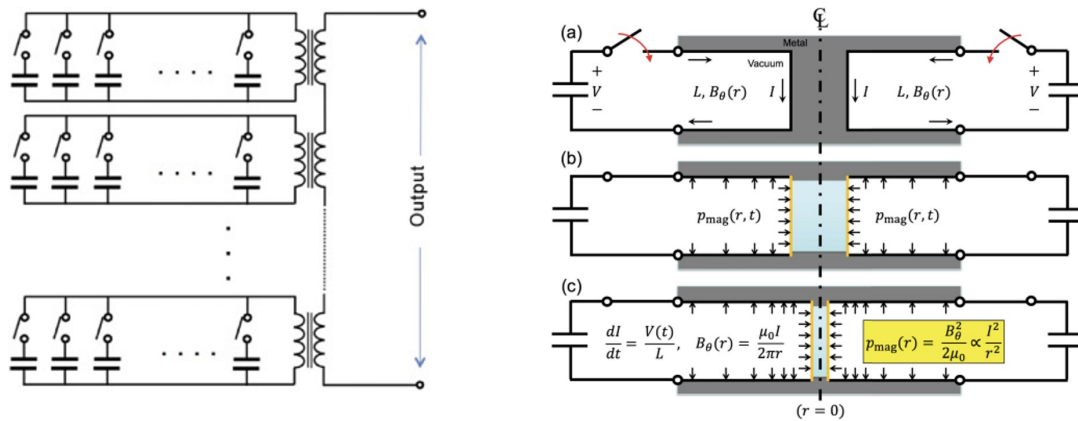


Figure 1: LTD architecture overview. Stacked cavities (left) and single brick (right). [1, 2]

2 Background and Theory

2.1 The Linear Transformer Driver

An LTD consists of one or more annular cavities, each containing a ring of capacitor-switch pairs called bricks. The bricks discharge in parallel into a one-turn primary around a ferromagnetic core. The core induces voltage on a central conductor. When multiple cavities are stacked, their voltages add along the conductor [1].

Terminology used in this report [1, 3]:

- **Brick** — two capacitors arranged symmetrically around one switch
- **Module** — one complete energy-storage unit
- **Cavity** — a ring of modules sharing a common core
- **Parallel configuration** — bricks in parallel sum their currents
- **Series stacking** — cavities in series sum their voltages

2.2 LTD vs. Marx Generator

Table 1: Comparison of LTD and Marx generator architectures.

	LTD	Marx Generator
Voltage addition	Magnetic, via cores	Series capacitors
Inductance	Low	High
Rise time	Fast (tens of ns)	Limited by stack inductance
Modularity	Excellent	Limited

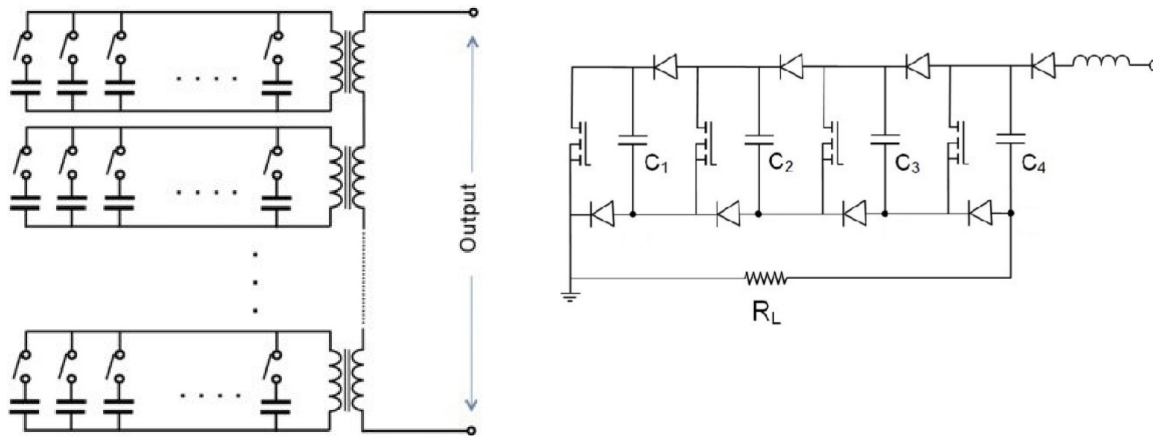


Figure 2: Solid-state Marx (right) and solid-state LTD (left) compared. [5, 2]

2.3 Solid-State vs. Gas-Switched LTDs

Industrial LTDs often use gas spark gaps, which can carry very high currents. However, they have drawbacks: electrode erosion limits lifetime, gas recovery limits repetition rate, and timing jitter is several nanoseconds. They also need gas handling equipment [4].

Solid-state switches trade some peak power for better performance in other areas:

Table 2: Spark-gap vs. solid-state switching.

	Gas Spark Gap	SiC MOSFET
Peak power	Very high	Moderate
Repetition rate	Low	High
Timing jitter	Several ns	Sub-ns
Maintenance	High	Minimal
Lifetime	Limited	Long

For a compact, repetitive lab driver, the solid-state approach is better [2, 3].

3 System Design

3.1 Top-Level Architecture

The prototype has one LTD stage with several bricks. Each brick has two ceramic capacitors and one SiC MOSFET, plus a freewheel diode and snubber. The bricks share a single-turn primary around a toroidal core.

The trigger chain is isolated from the high-voltage stage. An FPGA generates the timing waveform and drives an optical transmitter. At each brick, an optical receiver converts the signal back and feeds a gate driver.

Brick V1 schematic is shown in Figure 3.

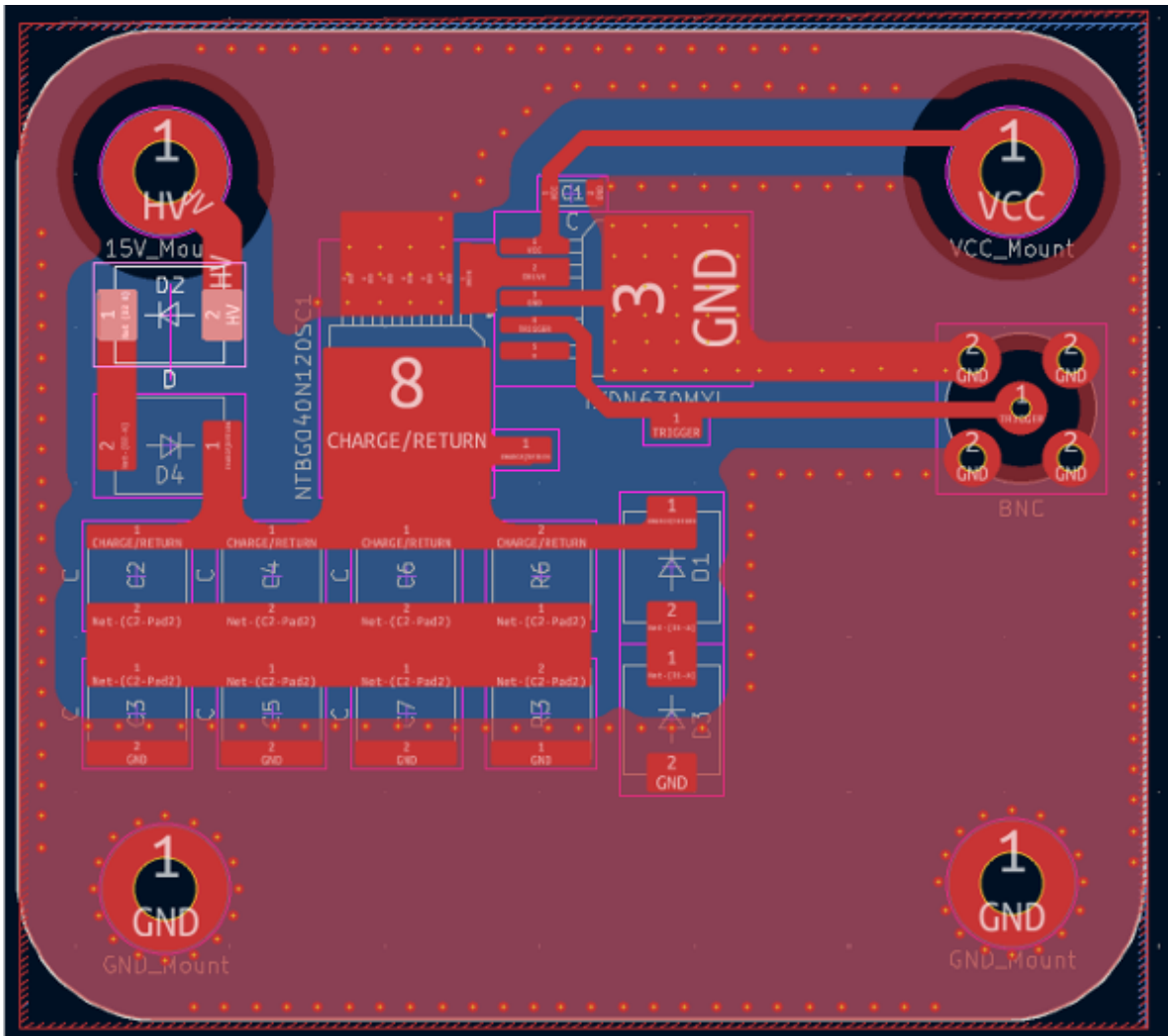


Figure 3: Brick V1 schematic diagram.

3.2 Capacitor and Switch Selection

3.2.1 Capacitors

The brick capacitor must store energy, deliver it quickly, and survive many discharges. Key requirements are low equivalent series resistance (ESR), low equivalent series inductance (ESL), and good pulse lifetime [1, 3]. The brick uses two MLCCs in a symmetric layout. Using many small capacitors in parallel gives lower inductance and better current sharing than one large capacitor.

Energy per discharge:

$$E_{\text{brick}} = \frac{1}{2} C_{\text{eq}} V_0^2 \quad (1)$$

3.2.2 SiC MOSFET Selection

SiC MOSFETs were chosen over silicon IGBTs for better high-voltage switching performance [6]. The selected device is an onsemi NTB040N120SC1.

Table 3: SiC MOSFET key parameters.

Parameter	Value
Drain-Source Voltage	1200 V
Pulsed Drain Current	240 A
Gate Charge	106 nC
Package	4-pin with Kelvin source

The Kelvin pin separates the gate return from the high-current source path, reducing switching loss and improving performance [7].

3.3 Gate Drive and Snubber Network

3.3.1 Gate Driver

The IXDN630MYI gate driver provides a low-impedance current source for the MOSFET gate, ensuring fast turn-on.

3.3.2 Flyback Diode

When the MOSFET turns off, any inductance in the circuit tries to keep current flowing. Without a path, this causes a voltage spike. The flyback diode provides a recirculation path. Adding this diode made a big improvement in waveform quality.

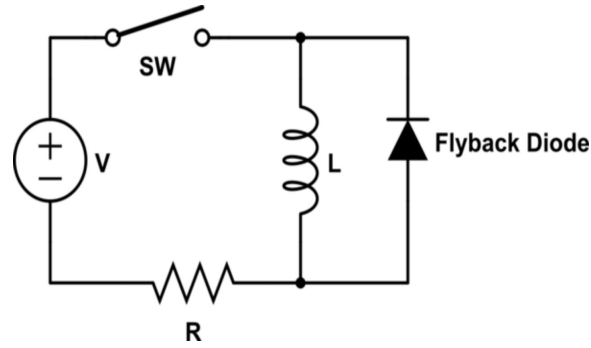


Figure 4: Flyback diode topology.

3.3.3 Snubber Circuit

A snubber across the MOSFET absorbs energy from parasitic inductance. It reduces voltage spikes and damps ringing. The snubber also helps parallel bricks stay synchronized.

We sized the snubber using a standard procedure: measure the natural ringing frequency, add a test capacitor, measure the shifted frequency, then calculate the needed R and C values.

Seven steps to calculate an R-C snubber	
Step 1	Measure the circuit's oscillation frequency (f_0). See Figure 1 (top).
Step 2	Add a capacitor (C_1) in parallel with the rectifier or FET and measure the shifted oscillation frequency (f_1). Select a C_1 value that is several times larger than the rectifier's stated typical capacitance at full-reverse voltage in the data sheet. In this example, the rectifier's reverse capacitance is 22pF, so I chose a 100pF value for C_1 . A frequency shift of at least 50% is reasonable. See Figure 1 (bottom).
Step 3	Calculate the frequency shift ratio: $m = \frac{f_0}{f_1}$.
Step 4	Calculate the circuit's parasitic capacitance: $C_0 = \frac{C_1}{(m^2-1)}$.
Step 5	Calculate the circuit's parasitic inductance: $L = \frac{(m^2-1)}{(2\pi f_0)^2 C_1}$.
Step 6	Calculate the starting snubber capacitor value: $C_{snub} = 3 * C_0$.
Step 7	Calculate the starting snubber-resistor value: $R_{snub} = \sqrt{\frac{L}{C_0}}$.

Figure 5: Snubber sizing procedure.

3.4 Magnetic Core Considerations

The core is driven around its hysteresis loop. Important properties are saturation flux density B_{sat} , retentivity B_r , and coercivity H_c .

To maximize flux swing, we need reset pulses between shots. Without reset, the core would only use half its range and would saturate after a few pulses [4].

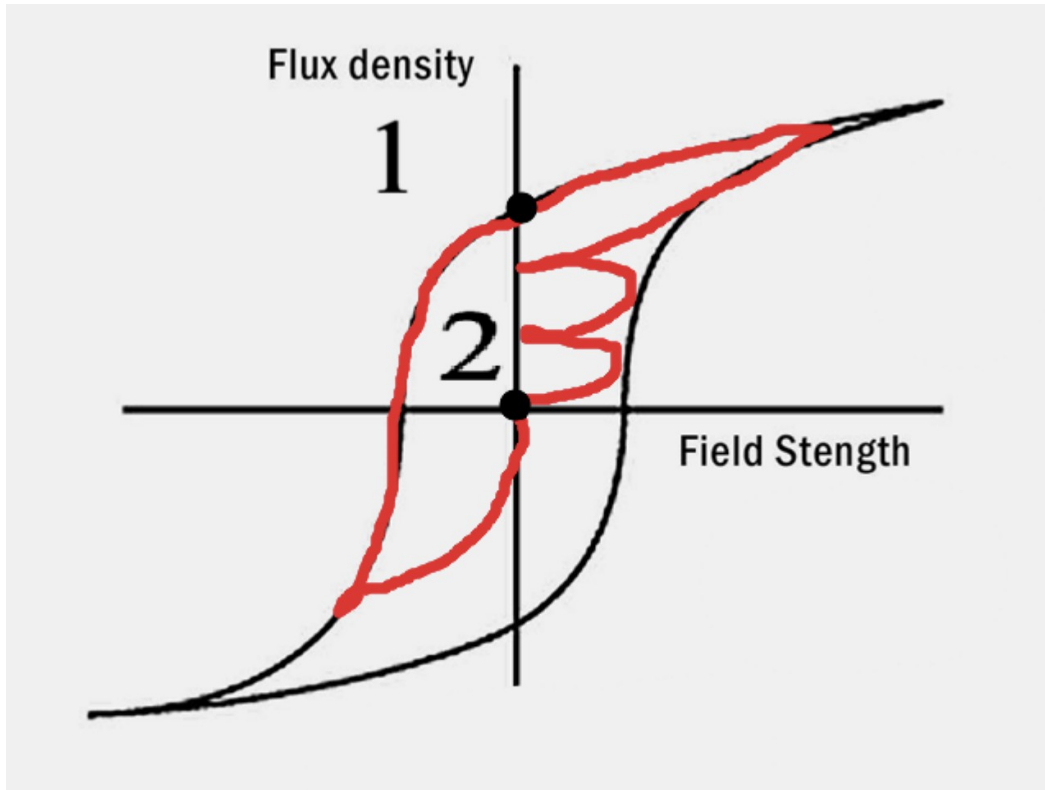


Figure 6: Magnetic core operating strategy with reset pulses.

3.5 Trigger Distribution

The trigger chain uses an FPGA driving fiber optics. Fiber gives complete electrical isolation and immunity to electromagnetic interference.

FPGA Pulse Generator

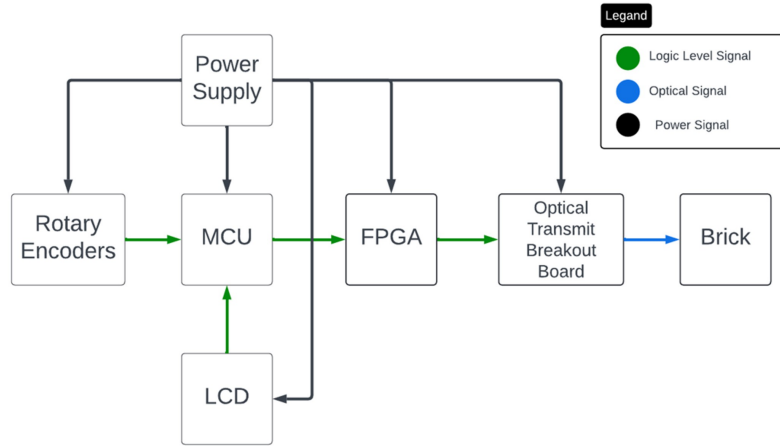


Figure 7: Trigger and control block diagram.

3.5.1 FPGA vs. Microcontroller

An FPGA was chosen over a microcontroller for deterministic timing and true parallel outputs. LTD performance depends on bricks firing at the same time, so sub-nanosecond synchronization is important.

3.5.2 Fiber-Optic vs. Coaxial Cable

Fiber provides galvanic isolation and is immune to EMI. Coaxial cable shares ground between controller and brick, so ground bounce and noise can cause false triggers.

3.5.3 Fiber-Optic Component Selection

Table 4: Fibre-optic trigger chain components.

Function	Part	Key Specs
FPGA platform	Digilent Artix-7	5 V supply
Optical Tx	Broadcom HFBR-1521Z	3.3–5 V supply
Optical Rx	Broadcom HFBR-2521Z	5 V supply
Optical fibre	Broadcom HFBR-RNS001Z	POF, 820 nm

3.6 PCB Layout

The PCB uses via fencing around high-current traces to reduce parasitic inductance [9, 10]. The layout is symmetric so the two capacitor paths have equal inductance. Asymmetric layout causes ringing and uneven current sharing.

Brick V1 - Board

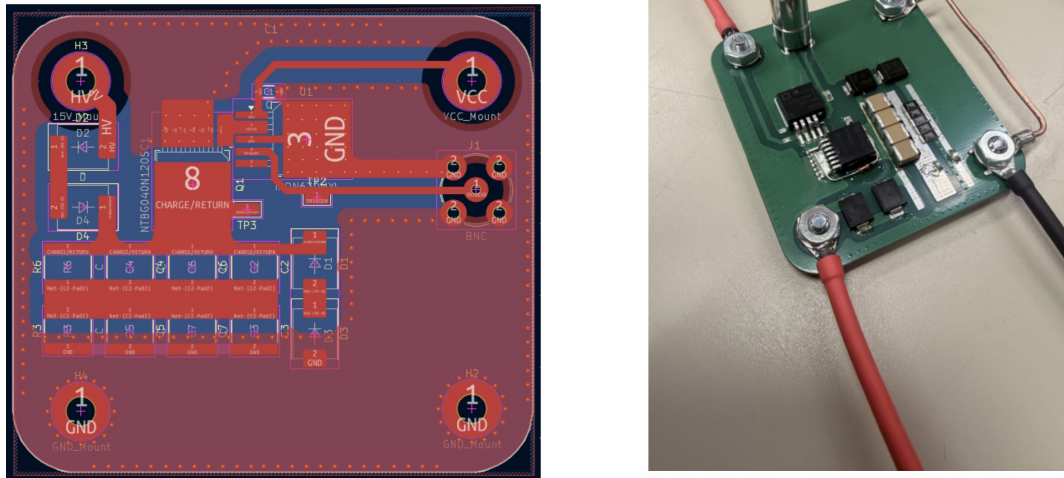


Figure 8: Brick V1 PCB layout (left) and assembled board (right).

4 Standards of Practice

The system was designed following:

- IEC 61010 — safety for electrical lab equipment [11]
- IEEE 510 — safety for high-voltage testing [12]
- IEC 61169-8 — BNC connector specifications [13]
- ASTM A773 — magnetic core characterization [14]
- IEC 60076 — power transformer requirements [15]

5 Results

Tests were done on a resistive load at about 100 V.

5.1 First Shot — Bare Brick

The board worked on first power-up, confirming the gate drive, MOSFET, and capacitors were all functional. However, rise time was 19.56 ns, slower than desired. The waveform had significant ringing.

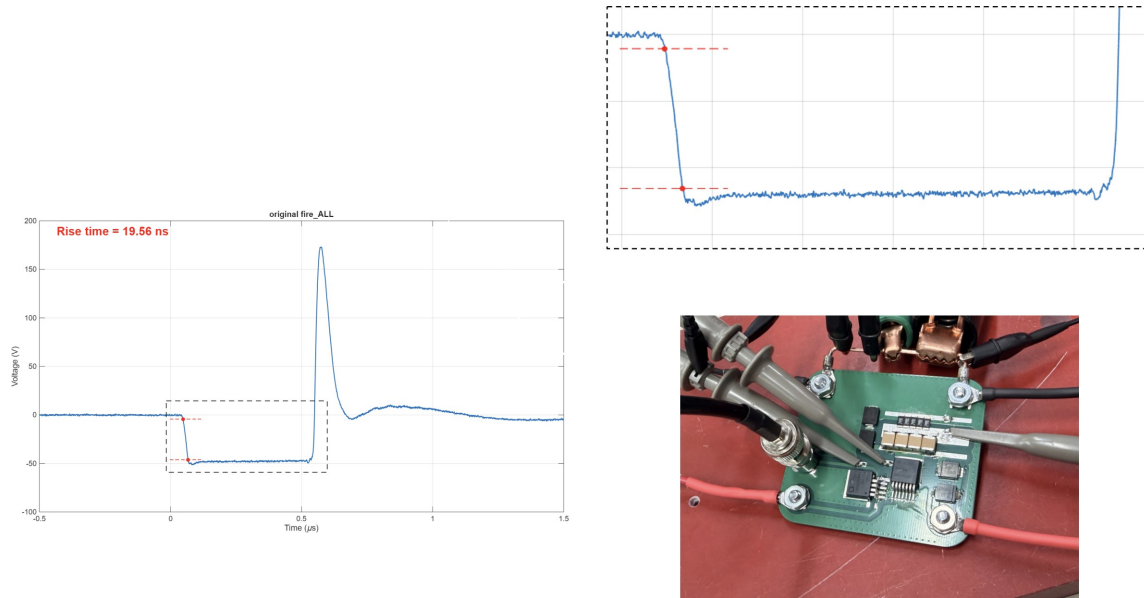


Figure 9: First-shot waveform of bare brick.

5.2 Adding the Flyback Diode

Adding the flyback diode made a dramatic improvement. Rise time dropped from 19.56 ns to 3.37 ns. Fall time measured 5.49 ns. The leading edge became much cleaner. Some ringing remained on the trailing edge.

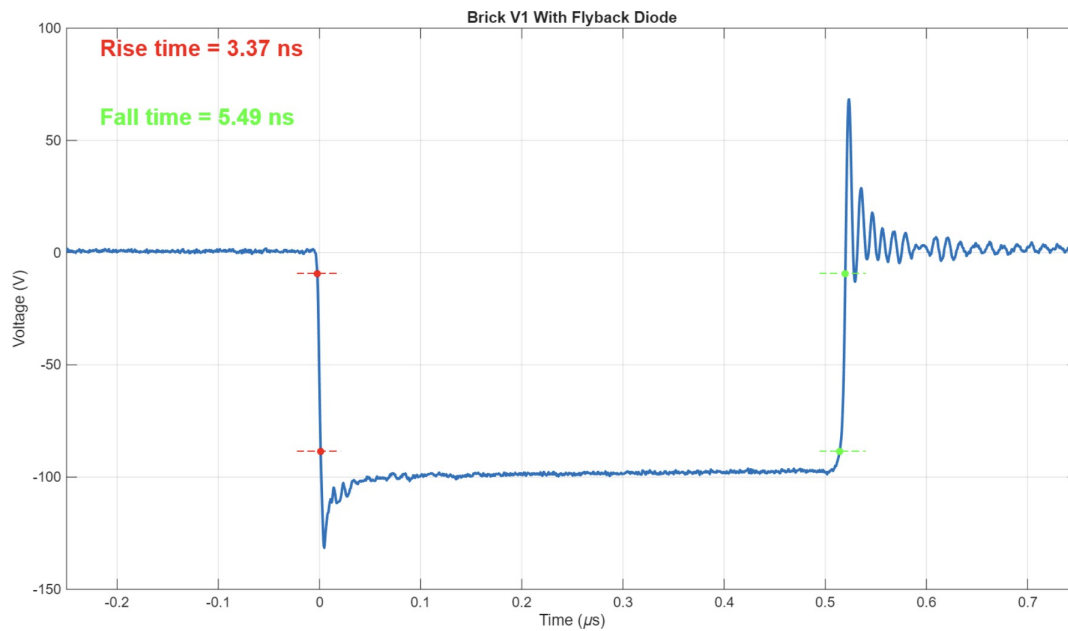
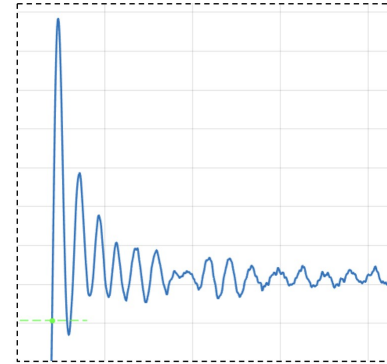
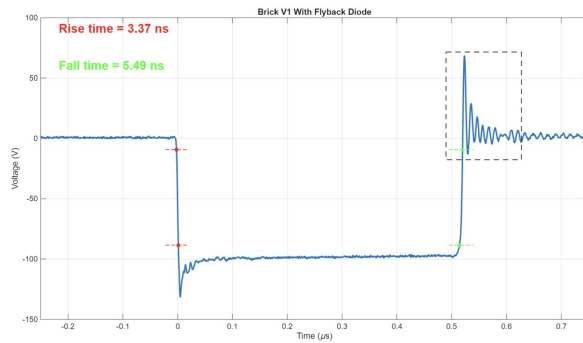


Figure 10: Waveform after adding flyback diode.

5.3 Snubber Calculation from Measured Ringing

We measured the trailing-edge ringing frequency at 91.26 MHz.



$$\Delta t_0 = 10.59 \text{ ns}$$

$$f_0 = 91.26 \text{ MHz}$$

Figure 11: Measuring the natural ringing frequency.

A 1 nF test capacitor was added across the MOSFET. The shifted ringing frequency gave us the parasitic L and C values, from which we calculated the snubber values.

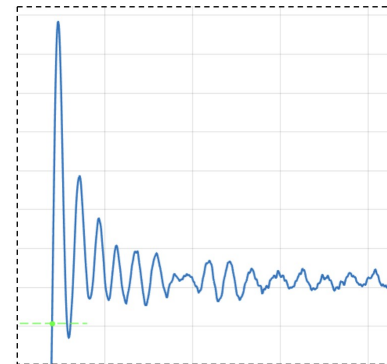
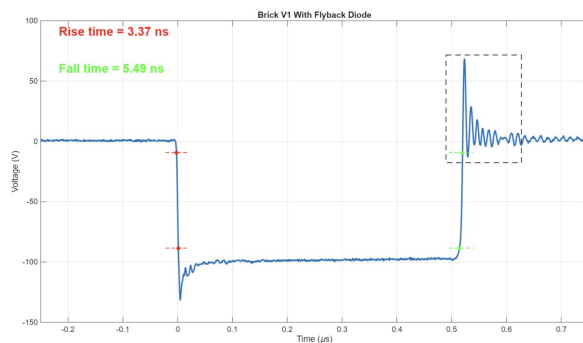


Figure 12: Frequency shift with test capacitor added.

5.4 Snubber Installation

Brick V1 did not have a snubber footprint initially, so we soldered through-hole R and C parts onto test pads. This works but lead inductance reduces effectiveness at high frequencies.

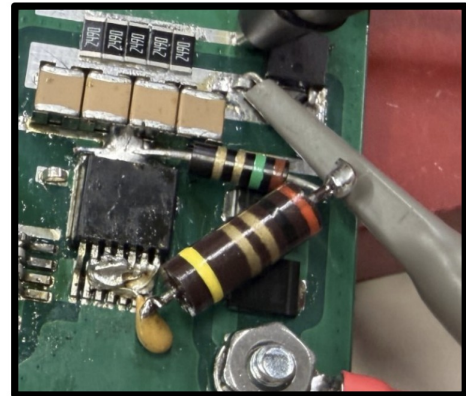
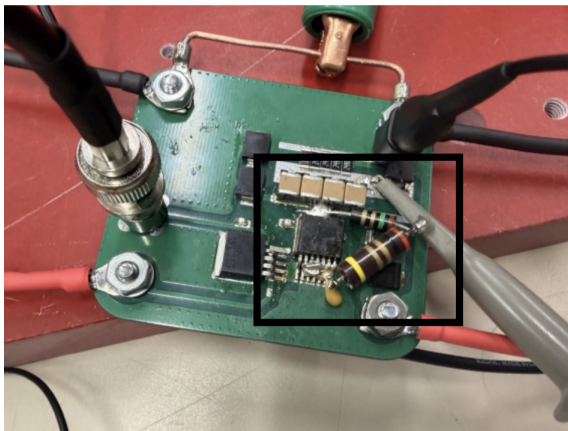


Figure 13: Through-hole snubber installed on Brick V1.

5.5 Final Waveform

With both flyback diode and snubber installed, the trailing-edge ringing was largely eliminated. Rise time was 11.24 ns and fall time was 10.96 ns. The snubber slowed the edge slightly compared to flyback-only, but this is expected and the trade-off was worth it for the cleaner pulse.

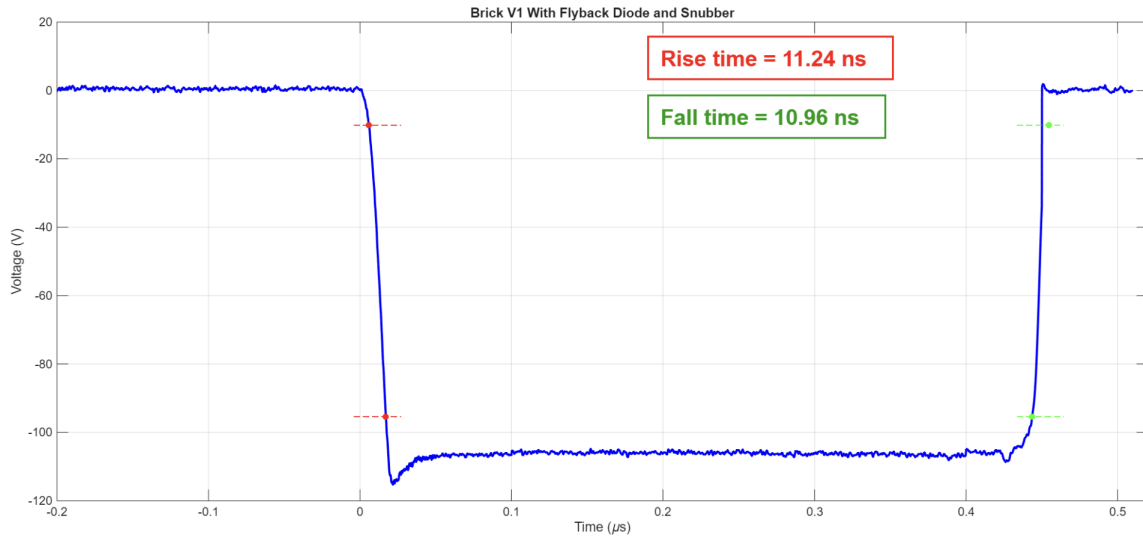


Figure 14: Final waveform with flyback diode and snubber.

5.6 Summary of Iterations

Table 5: Measured performance across design iterations.

Configuration	Rise (ns)	Fall (ns)
Bare brick	19.56	—
+ Flyback diode	3.37	5.49
+ Flyback + snubber	11.24	10.96

5.7 Brick V2

We designed a revised board (Brick V2) with an integrated snubber footprint, opto-isolated trigger input, and better flyback diode placement. It was ordered at the end of the semester.

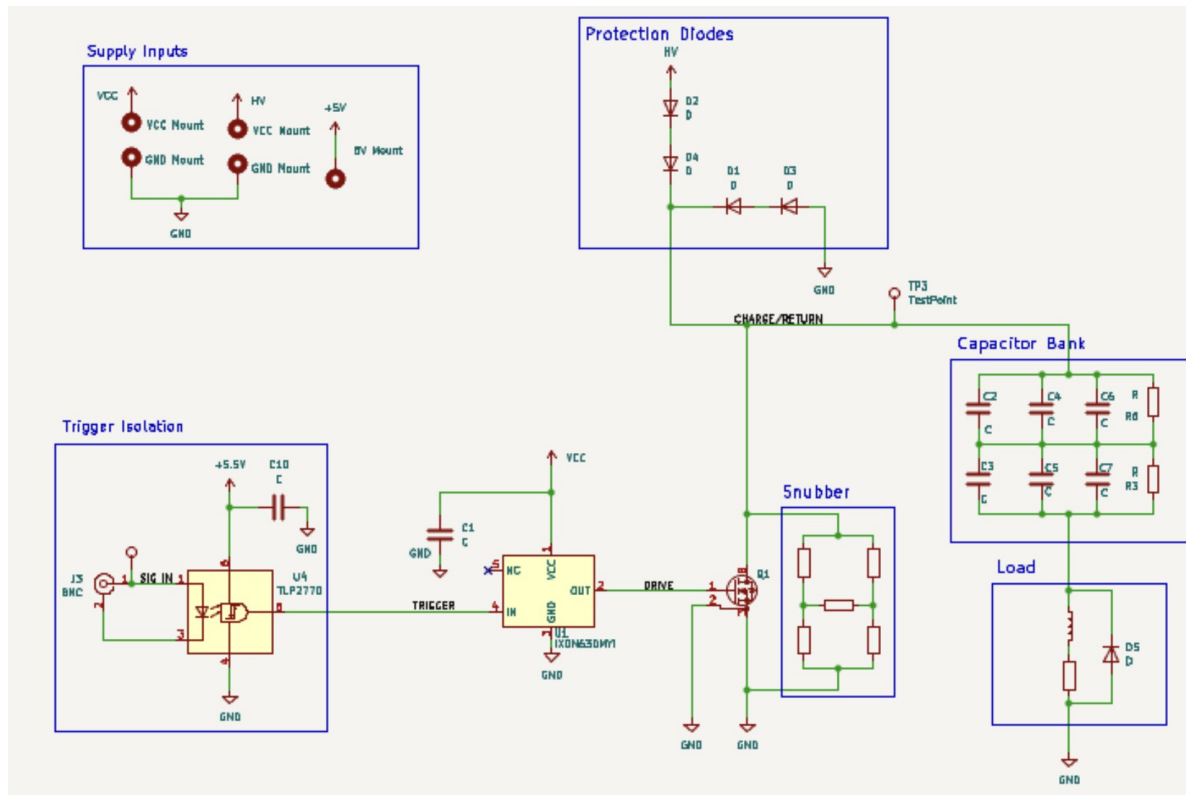


Figure 15: Brick V2 schematic diagram.

6 Applications

Compact LTDs are useful for:

- Plasma-based wastewater treatment
- Pulsed electric field food processing
- Sterilization using electron beams
- Defense and aerospace testing (EMP effects)

The same architecture appears at very different scales, from benchtop demonstrators to multi-megaampere fusion drivers.

7 Project Management

7.1 Bill of Materials

Table 6: Bill of materials for a single brick.

Item	Qty	Unit (\$)	Ext. (\$)
BNC connector	3	5.64	16.92
Gate driver	3	9.11	27.33
SiC MOSFET	3	18.82	56.46
Ceramic capacitors	10	2.87	28.70
Rectifier diode	10	0.67	6.74
Resistors	20	0.53	10.62
Test points	20	0.36	7.20
PCB	1	12.67	20.89
Total			\$174.86

8 Challenges and Future Work

8.1 Remaining Challenges

- Parasitic inductance in high-current traces still limits rise time
- Core heating at high repetition rates
- PCB fabrication lead times drove the schedule

8.2 End-of-Semester Status

By the end of the semester, we achieved:

- Brick V1 designed, built, and tested on a resistive load
- Three measurement iterations completed
- Snubber values derived experimentally
- Brick V2 designed and ordered
- FPGA code written and fiber breakout designed

8.3 Future Work

- High-voltage test of a single brick
- Multi-brick parallel operation
- Full multi-stage cavity design

9 Conclusion

This project produced a working solid-state LTD brick. The combination of SiC MOSFET switching, fiber-optic trigger isolation, and careful PCB layout worked as intended. Measured rise times improved from 19.56 ns on first shot to 3.37 ns after adding the flyback diode, with the final snubbed configuration at 11.24 ns rise and 10.96 ns fall while eliminating most ringing.

The key lesson is that at pulsed-power timescales, physical layout matters as much as the schematic. Via fencing, symmetric capacitor placement, the Kelvin pin, and fiber-optic isolation all made significant differences.

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